

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Donald F. Hooper, et al. Art Unit: 2155
Serial No.: 09/626,535 Examiner: David Y. Eng
Filed : July 27, 2000
Assignee : Intel Corporation
Title : MULTI-THREADED SCHEDULED RECEIVE FOR FAST NETWORK
PORT DATA

MAIL STOP RCE

Commissioner for Patents
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Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicants call attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

This filing is being made with a Request for Continued Examination. No fee is required.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

Please apply any credits or additional charges to deposit account 06-1050.

Respectfully submitted,

Date: March 20, 2007

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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-137002	Application No. 09/626,535
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Donald F. Hooper, et al.	
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U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2004/0073778	04/2004	Adiletta et al.			
	AB	3,373,408	03/1968	Ling			
	AC	3,478,322	11/1969	Evans			
	AD	3,792,441	02/1974	Wymore et al.			
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	AZ	5,404,482	04/1995	Stamm et al.			
	BA	5,432,918	07/1995	Stamm			

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	BK	5,544,236	08/1996	Andruska et al.			
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	DD	5,937,187	08/1999	Kosche et al.			
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	EK	6,201,807	03/2001	Prasanna			
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	FJ	6,430,626	08/2002	Witkowski et al.			
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	FL	6,463,072	10/2002	Wolrich et al.			
	FM	6,532,509	03/2003	Wolrich et al.			
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	FW	6,667,920	12/2003	Wolrich et al.			
	FX	6,668,317	12/2003	Bernstein et al.			
	FY	6,681,300	01/2004	Wolrich et al.			
	FZ	6,694,380	02/2004	Wolrich et al.			

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	GA	0 379 709	08/1990	EPO				
	GB	0 464 715	01/1992	EPO				
	GC	0 633 678	01/1995	EPO				

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Foreign Patent Documents or Published Foreign Patent Applications

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							Yes	No
	GD	0 745 933	12/1996	EPO				
	GE	0 809 180	11/1997	EPO				

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	GF	Byrd et al., "Multithread Processor Architectures," <i>IEEE Spectrum</i> , 32(8):38-46, New York, August 1995.
	GG	Doyle et al., <i>Microsoft Press Computer Dictionary</i> , 2 nd ed., Microsoft Press, Redmond, Washington, USA, p. 326, (1994).
	GH	Fillo et al., "The M-Machine Multicomputer," <i>IEEE Proceedings of MICRO-28</i> , pp. 146-156, (1995).
	GI	Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," <i>Journal of Parallel and Distributed Computing</i> , Academic Press, Duluth, Minnesota, USA, 40(1):103-117, January 1997.
	GJ	Haug et al., "Reconfigurable hardware as shared resource for parallel threads," <i>IEEE Symposium on FPGAs for Custom Computing Machines</i> , 2 pages, (1998).
	GK	Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," <i>Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines</i> , pp. 12-21, (1997).
	GL	Hyde, R., "Overview of Memory Management," <i>Byte</i> , 13(4):219-225, (1988).
	GM	Litch et al., "StrongARMing Portable Communications," <i>IEEE Micro</i> , pp. 48-55, (1998).
	GN	Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, <i>Online!</i> , 13 November 1998, pages 1-19.
	GO	Thistle et al., "A Processor Architecture for Horizon," <i>IEEE Proc. Supercomputing '88</i> , pp. 35-41, (1988).
	GP	Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," <i>IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences</i> , pp. 191-201, (1995).
	GQ	Trimberger et al., "A time-multiplexed FPGA," <i>Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines</i> , pp. 22-28, (1997).
	GR	Turner et al., "Design of a High Performance Active Router," Internet Document, <i>Online!</i> , 20 pages, 18 March 1999.
	GS	Wazlowski et al., "PRSIM-II computer and architecture," <i>IEEE Proceedings, Workshop on FPGAs for Custom Computing Machines</i> , pp. 9-16, (1993).
	GT	U.S. Patent Application No. 09/473,571, filed December 28, 1999, Wolrich et al.
	GU	U.S. Patent Application No. 09/475,614, filed December 30, 1999, Wolrich et al.

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